A Low-Power and Variable-Gain Transceiver Front-End Chip for 5-GHz-Band WLAN Applications

Hideaki Dodo, Yuuichi Aoki, Nobuyuki Hayama, Masahiro Fujii, Yuu Yamaguchi*, Yasuhumi Sasaki*, Hideo Ohba*, and Hikaru Hida

Photonic and Wireless Device Research Labs., NEC Corporation, 34 Miyukigaoka, Tsukuba, Ibaraki 305-8501, Japan

*1st Custom LSI Division, NEC Electronics Corporation, 1753 Shimonumabe, Nakahara, Kawasaki, Kanagawa 211-8666, Japan

***ABSTRACT* — A low-power 5-GHz-band transceiver front-end chip is described that uses highly reliable, high-performance InGaP/GaAs HBTs and complies with IEEE802.11a standards. Integrated into the chip (2.4×2.4 mm^2) are a 20/0-dB dual-gain low-noise amplifier and a wide IF-range down-conversion mixer in the receiver path, a 20-dB variable-gain driver amplifier and a low and stable local oscillator (LO) leakage up-conversion mixer in the transmitter path, and a high-isolation LO buffer. Very low power consumption (120 mW) is attained with a single 3-V supply voltage in receiver mode together with high transceiver performance. The key features and new circuit approaches in each function block are described in details. Measurement showed that a 5-GHz OFDM-modulated Tx signal meets IEEE802.11a standards.**

I. INTRODUCTION

Wireless local area networks (WLANs), which are becoming common in homes and offices as well as in hot spot areas, commonly use 2.4-GHz ISM-band wireless LAN systems like IEEE802.11b. Newer 5-GHz WLANs systems based on orthogonal frequency division multiplexing (OFDM) modulation, such as defined in IEEE 802.11a and used in HiperLAN2, are more attractive due to their high data rates, e.g., 54 Mbps, and robustness in multipath fading environments. Recent activities that relax regulations restricting outdoor usage of these systems should expand their market size.

A key issue in their acceptance is the development of transceivers (TRx) with lower power consumption and lower cost. RF-TRx ICs for 5-GHz-band wireless systems using BiCMOS, CMOS, and SiGe technology have been reported [1-5]. However, to the best of our knowledge, there have been no reports on a one-chip TRx front-end IC that complies with IEEE 802.11a standards. The main obstacle to development is the strict linearity requirements for OFDM signals.

We have developed a 5-GHz-band transceiver front-end chip that complies with IEEE 802.11a standards. New circuit design approaches are used to achieve various functions, robustness over interference, and low power consumption.

II. Circuit Design

Figure 1 shows a block diagram of the 5-GHz-band transceiver front-end chip. It is composed of a low-noise amplifier (LNA) and a down-conversion mixer in the receiver path, a driver amplifier and an up-conversion mixer in the transmitter path, and a local oscillator (LO) buffer. The chip operates at a single voltage of 3 V and has a shut-down mode; that is, the transmitter path is shut down when the receiver path is in use, and vice versa.

A. LNA

A wide dynamic range LNA has two-stage amplifier configuration with dual gain mode. The first stage is a cascode amplifier, and the second is composed of two path circuits., One is a high-gain path using an HBT amplifier, and the other is an attenuation path using a resistor. The mode is switched by externally controlling the base-bias voltages of two common-base-HBT amplifiers placed in parallel in the first stage. A low noise figure (NF) is required in the high-gain mode to maximize signal sensitivity; it is achieved by using the high-gain cascode amplifier. A high handling power capability is required in both modes; it is represented by the input referred 1-dB compression point (P1dB). This capability is achieved by suppressing P1dB degradation in the second stage, which is done by operating the low-resistance bias-feed resistor of the HBT amplifier in high-gain mode and by operating the attenuation resistor in attenuation mode [6]. Simulation showed that operation of the chip in high- (low-) gain mode produced an NF of 2.6 dB (3.8 dB), a gain of 21.3 dB (1.8 dB), and a P1dB of −10.8 dBm (−5.3 dBm).

0-7803-7695-1/03/$17.00 © 2003 IEEE

2003 IEEE MTT-S Digest

B. Driver Amplifier

The two main functions of the driver amplifier are to amplify the up-conversion signals and to drive the power amplifier. It also has a variable gain feature that suppresses gain fluctuations due to variations in operating temperature and frequency in the transmitter path. It consists of a two-stage amplifier, a diode-loaded emitter follower attenuation circuit, and a simple on-chip LC filter for direct connection with the up-conversion mixer. By controlling both the base-bias of the second-stage HBT and that of the attenuation circuit, a gain control range of more than 20 dB is achieved, as shown in Table I. The basic variable gain scheme was reported in our previous work [8].

C. Down- and up-conversion mixer

Both the down- and up-conversion mixers are designed to operate in a wide IF frequency range (about 1 GHz) to enable the use of a wide variety of IF frequencies. The mixers are composed of a Gilbert cell with resistive loading and a push-pull output amplifier, as shown in Fig. 2. The push-pull amplifier transforms the differential output into a single output in the wide IF frequency range. Its configuration enables it to obtain high gain with much lower current consumption.

In the down-conversion mixer, an emitter degeneration spiral inductor is used in the Gilbert cell to improve linearity without degrading the NF.

In the up-conversion mixer, an impedance-matching resistor (RR), see Fig. 2, is newly introduced to reduce and stabilize the LO leakage. Simulation showed that LO leakage is very sensitive to fluctuations in the inductance of bonding wire (LL) connected to a large external chip capacitor (CC) because it degrades the differential operation of the IF input HBT pairs (Fig. 3). It also showed that a matching resistance of about 50 Ω results in both small LO leakage and weak dependence of it on the inductance fluctuation. The simulated results are summarized in Table I.

D. LO buffer

An LO buffer is needed to increase the isolation between the LO inputs of the two mixers and an external VCO output and to stabilize the LO frequency when switching between mixers. The LO buffer is composed of two cascaded differential amplifiers and an output emitter follower.

III. Chip Performance

The TRx front-end chip was fabricated using a highly reliable InGaP/GaAs HBT process [7]. A microphotograph of the chip is shown in Fig. 4. The chip is 2.4×2.4 mm^2 and was assembled in a 44-pin-QFN package. The evaluation conditions were 5.25-GHz RF frequency, 500-MHz IF frequency, 3-V supply voltage, and −6-dBm LO power. The simulation and measurement results for each function block are summarized in Table I. There was good agreement.

Figure 5 shows the gain and NF of the LNA. In high-gain mode, a high gain of over 20 dB and a low NF of about 2.7 dB were achieved at around 5 GHz. In low-gain mode, 21-dB step gain attenuation was achieved, leading to avoiding linearity degradation at high input-signal power levels.

Figure 6 shows the dependence of the output power attenuation of the variable-gain driver amplifier on the control voltage. The IF input power was −20 dBm through the up-conversion mixer. A large gain variation of 25 dB was achieved by increasing the control voltage from 1 to 2 V. The total gain of both the driver amplifier and the up-conversion mixer was 15 dB in full-gain mode.

Figure 7 shows the down-conversion-mixer gain dependence on the IF frequency. The gain degradation was very small, less than 1.5 dB, demonstrating that this chip can be used for a wide variety of IF frequencies. This mixer had a gain of 7.5 dB, an NF of 12.5 dB, and a P1dB of 0 dBm.

As shown in Fig. 3, the measured LO leakage of the up-conversion mixer was −22 dBm, which is sufficiently small compared with the 8-dBm output power of the up-conversion mixer. As explained in Sec. II, an impedance-matching on-chip resistance of 50 Ω reduces LO leakage and its fluctuation, and this results in high yields.

The transmission spectra of an OFDM-modulated 5-GHz RF signal shown in Fig. 8 shows that the adjacent channel penetration power ratio (ACPR) meets the specifications of the IEEE 802.11a standard.

IV. Conclusion

We have developed a low-power 5-GHz-band transceiver front-end chip using InGaP/GaAs HBTs that complies with IEEE802.11a standards. The small chip (2.4×2.4 mm^2) is composed of a LNA, up- and down-conversion mixers, a driver amplifier, and a LO buffer. Several new circuit design approaches were used to achieve lower power consumption (120 mW) in receive mode and to meet the high linearity requirement of the OFDM modulation scheme. This chip is thus suitable for use in IEEE 802.11a wireless local area network systems. Future work to further reduce power consumption and cost as well as to incorporate the multi-band/multi-mode functions will further expand the WLAN markets.

ACKNOWLEDGEMENT

The authors are grateful to the many engineers in the NEC Compound Semiconductor Devices, Ltd. who assisted with the chip fabrication. They also wish to thank T. Mochizuki, M. Mineo, M. Matsunoshita, Dr. H. Hirayama, and Dr. M. Mizuta for their valuable comments and encouragement throughout this work.

References

[1] M. Madihian, T. Drenski, L. Desclosi, H. Yoshida, H. Hirabayashi and T. Yamazaki, "A 5-GHz-band Multifunctional BiCMOS Transceiver Chip for GMSK Modulation Wireless Systems," IEEE. Journal of Solid-State Circuits, Vol. 34, No.1, pp. 25-32, 1999.

[2] M. Copeland, P. Voinigescu, D. Marchesan, P. Popescu, and M. Maliepaard, "A 5-GHz SiGe HBT Monolithic Radio Transceiver with Tunable Filtering," IEEE Transactions on Microwave Theory and Techniques, Vol. 48, No. 2, pp. 170-181, 2000.

[3] T-P. Liu and E. Westerwick, "5-GHz CMOS Radio Transceiver Front-End Chipset," IEEE. Journal of Solid-State Circuits, Vol. 35, No. 12, pp. 1927-1933, 2000.

[4] S. Yoo, D. Heo, C-H. Lee, B. Matinpour, S. Chacrabotry, and J. Laskar, "A 5.8 GHz OFDM GaAs MESFET MMIC Chip Set," IEEE. MTT-S Dig., pp. 1273-1276, 2000.

[5] J-O. Plouchart, H. Ainspan, and M. Soyuer, "A 5.2 GHz 3.3 V I/Q SiGe RF Transceiver," IEEE.1999 Custom Integrated Circuits Conference, pp. 217-220, 1999.

[6] Y. Aoki, N. Hayama, M. Fujii, and H. Hida, "A 23/3-dB Dual-Gain Low-Noise Amplifier for 5-GHz-Band Wireless Applications," 2002 IEEE, GaAs-IC Symp. Dig., pp. 197-200, 2002.

[7] H.Simawaki, "InGaP/GaAs HBTs for Portable Wireless Applications," Proceedings of the Topical Workshop on Heterostructure Microelectronics, pp.104, 2000

[8] Y. Aoki, M. Fujii, S. Ohkubo, S. Yoshida, T.Niwa, Y. Miyoshi, H. Dodo, N.Goto, and H.Hida, "A 1.4-dB-NF Variable-Gain LNA with Continuous control for 2-GHz-band Mobile Phones Using InGaP Emitter," 2001 IEEE RFIC. Symp. Dig, pp. 231-234, 2001.

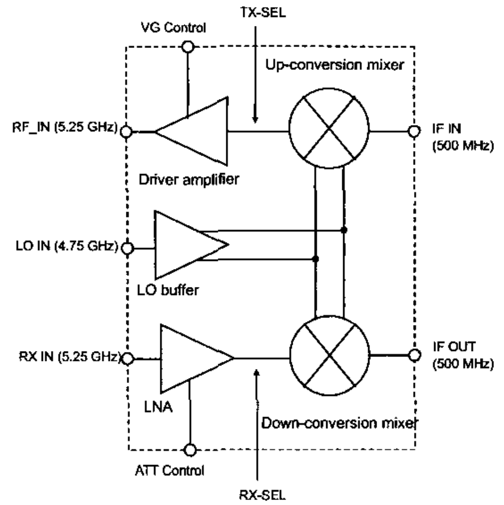

Fig. 1 Block diagram of transceiver front-end chip.

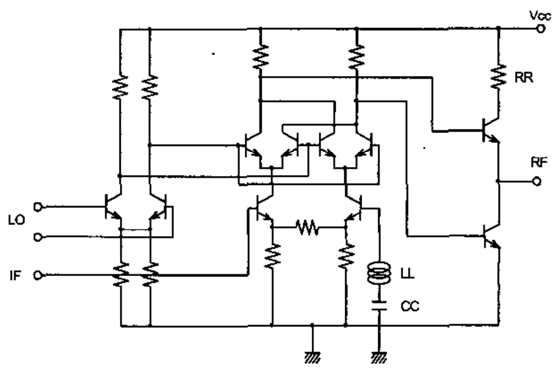

Fig. 2 Simplified circuit schematic of up-conversion mixer

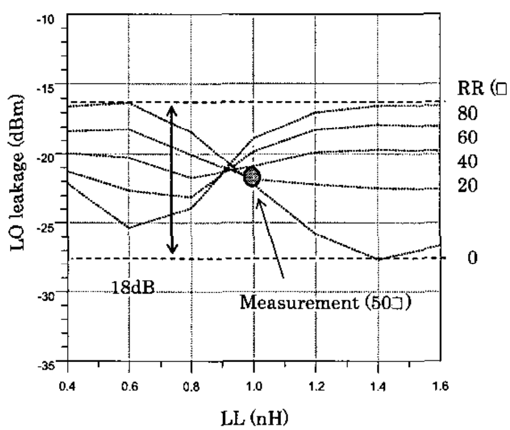

Fig. 3 External bonding-wire inductance (LL) and internal matching resistance (RR) dependences of LO leakage in up-conversion mixer. Lines represent simulated results.

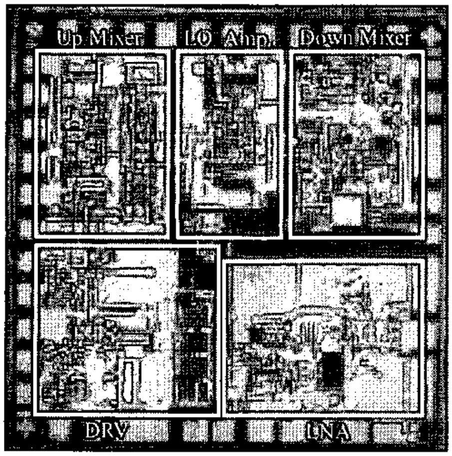

Fig. 4 Microphotograph of developed transceiver front-end chip (2.4×2.4 mm^2).

Table I. Simulation and measurement results for each circuit block @ RF=5.25 GHz, IF=500 MHz, LO=−6 dBm, and Vcc=3 V.

Circuit	Features	Simulation	Measurement
LNA	Gain (dB)	21.3	22
	Gain ATT (dB)	19.5	21
	NF (dB)	2.6	2.7
	I (mA)	14.1	14
Down Mixer	Gain (dB)	8	7.5
	NF (dB)	13	12.5
	P1dB (dBm)	3	0
	I (mA)	18	17
DRV+Up Mixer	Gain (dB)	17	15
	Gain ATT (dB)	22	25
	P1dB (dBm)	5	0
	LO leak (dBm)	−13	−15
	I (mA)	68	69
LO Buffer	I (mA)	10	10
Rx Total	I (mA)	41	41
Tx Total	I (mA)	78	79

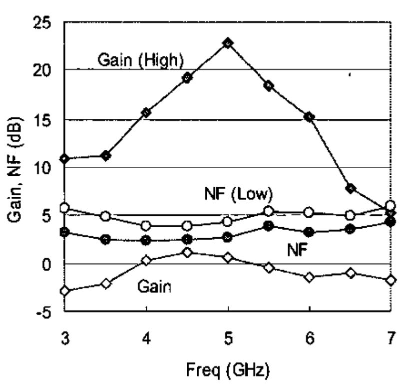

Fig. 5 Gain and NF of dual-gain LNA for high-gain and low-gain modes.

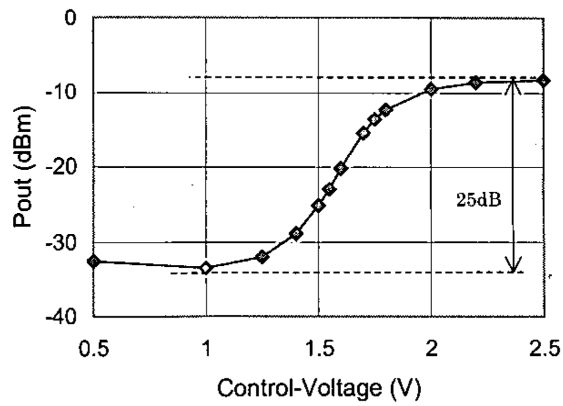

Fig. 6 Dependence of output power (Pout) attenuation of driver amplifier on control voltage. IF input power was −20 dBm through the up-conversion mixer.

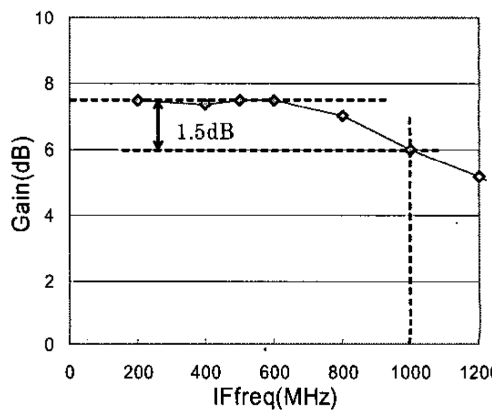

Fig. 7 Down-conversion-mixer gain dependence on IF frequency.

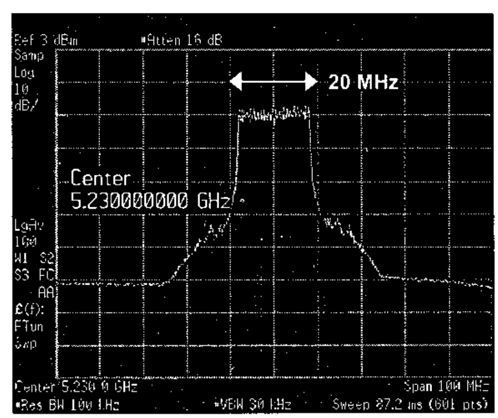

Fig. 8 Transmission spectra of OFDM-modulated 5-GHz RF signal.